REMARKS

In view of the Final office action of December 23, 2004, the foregoing amendments, and the following remarks, clarify differences between the immediate application and the cited prior art. Claim 21, dependent from claim 1, is added. Claims 1, 3 – 21 remain pending, of which claims 1 and 12 are independent. No new matter is added.

Claim 1 is amended to clarify cycle-based operation of the method, wherein: if the current cycle is not a checkpoint cycle, data from architected registers of the register file is stored in the buffer; if the current cycle is a checkpoint cycle, a check is made for data errors; and if data errors exist, registers of the register file are restored from the buffer. Support for these changes is found, at least, in paragraphs [0006] – [0007] and [0018] – [0022] of the specification.

Claim 12 is also amended for clarity.. For example, the buffer is recited as storing a copy of data within at least one, but not all, registers prior to loading the new data; and that the register data is restored to the register file in the event that data errors are detected at a checkpoint, wherein the buffer is flushed at the checkpoint if no data errors are detected. Paragraphs [0006] – [0007] and [0018] – [0022] again provide support for these amendments.

Claim 21 is added, depending from claim 1, to provide an example where the checkpoint occurs each plurality of processor cycles. Support for this new claim is found, at least, in paragraphs [0006] – [0007] and [0022] of the specification and in FIG. 2.

On the other hand, Bozso discloses a "method for detecting and correcting errors occurring in mirrored processors." See Bozso, col. 2 lines 24-28. Bozso specifically requires "two processors running identical code in lock-step." See Bozso col. 2, lines 29-31. In contrast, claims of the present application concern the recovery of data errors in a single processor. Further, Bozso makes a backup of all registers, not just those that are architected, as required, for example, by claim 1. In the present

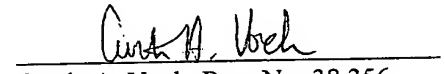
application, the buffer may have "a fraction of the memory capacity of the register file", for example "twenty registers as compared to one hundred twenty eight registers in the register file." See paragraph [0006] of the specification. This buffer is flushed when no errors are detected at a checkpoint, thereby emptying the buffer.

Contrary to the examiner's statement, the checkpointed state array of Bozso is not 'flushed' or emptied when the aggregate current state array is transferred to the checkpointed state array, since the action of transferring re-fills the checkpointed state array.

The present application clearly operates in a different manner to that of Bozso. Applicant therefore requests reconsideration and allowance of claims 1, 3-21.

Applicant believes no fees are due in connection with this Amendment and Response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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